Remarks

Claims 1-20 are pending in the application and stand rejected. Claims 1-15 would be allowable if rewritten to overcome the Examiner's rejection under 35 U.S.C. § 112, 2nd paragraph. By this response claims 1, 15, 16, 17 and 18 have been amended. Applicants respectfully request reconsideration of all pending claims herein.

Claim Rejections - 35 U.S.C. § 112

The Examiner rejected claims 1-15, 18 and 20 under 35 U.S.C. § 112, 2nd paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

In claim 1, the Examiner noted there is no antecedent basis for "the supply voltage." Accordingly, Applicants have amended claim 1 to correct this deficiency. Claims 2-14 depend from Claim 1 as amended. Therefore, the Examiner's rejection has been overcome and claims 1-14 are in condition for allowance.

In claim 15, the Examiner indicated there is no antecedent basis for "the second terminal" at lines 9-10. Accordingly, Applicants have amended claim 15 to recite "a second terminal" in lines 9-10. Therefore, the Examiner's rejection has been overcome and claim 15 is in condition for allowance.

In claim 16, the Examiner indicated that "a reference voltage" had previously been recited at line 5. Accordingly, Applicants have amended claim 15 to recite "the reference voltage" at lines 6-7. Claims 16-18 depend from claim 15 as amended. Therefore, the Examiner's rejection has been overcome and claims 15-18 are in condition for allowance.

In claim 18, the Examiner indicated there is no antecedent for "the plurality of electronic fuses." Accordingly, Applicants have amended claim 18 to recite "a plurality of electronic fuses"

to overcome the Examiner's rejection.

The Examiner stated that no support is found in the specification for "comparing the voltage drop across each of the plurality of electronic fuses..." Applicants respectfully submit that Figs. 3-4 illustrate a gating transistor mN[j] for each of the plurality of electronic fuses xF[j]. In addition, Fig. 7A and 7B illustrate an exemplar schematic of the additional logic required for fuse selection and sensing. Applicants' specification at paragraph 37 further describes the steps necessary for fuse sensing and selection. In order to more distinctly claim the subject matter herein, Applicants have amended the comparing step of claim 18 to state that "each of the plurality of electronic fuses is sensed independently." Accordingly, Applicants respectfully submit that the Examiner's rejection of claims 16-18 and 19-20 has been overcome.

Claim Rejections - 35 U.S.C. § 102(b)

The Examiner rejected claims 16-20 under 35 U.S.C. § 102(b) as being anticipated by U.S Patent No. 6,011,428 to Tsukude et al. The Examiner stated that Tsukude discloses similar elements corresponding to the limitations of Applicants' method steps recited in independent claim 16 but directed to laser programming of optical fuses.

Conversely, Applicants' method is directed to electronically programmable eFuses using low voltage and a differential sensing scheme. Applicants respectfully submit that Tsukude does not anticipate or suggest Applicants recited method because Tsukude is directed to a fundamentally different fuse technology that is employed to realize a temperature compensated voltage level shifter circuit. Moreover, the surrounding circuit structure shows a common control signal /VDCEP applied to the gates of each of transistors 600-60n, which would preclude individual sensing of the fuse element. Instead, the Tsukude fuse elements are incorporated in a resistor network as a way to overcome semiconductor process manufacturing variations and adjust the output of the level shifter once the device has been characterized during wafer test. (Tsukude, Col. 12, lines 64-67 and Col. 13, lines 1-31. As such, Applicants respectfully submit that the method claimed herein is not anticipated or suggested by Tsukude.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. (MPEP §2131) Applicants respectfully submit that Tsukude does not teach or suggest Applicants' method of programming and sensing an electronically programmable eFuse. Although Tsukude does not anticipate every element of Applicants' claimed method, Applicants have amended claim 16 to recite "a method of programming and sensing the state of a voltage programmable electronic fuse (eFuse) in an integrated circuit..' Claims 17-20 depend from claim 16. Therefore, Applicants respectfully submit that the Examiner's rejection of claims 16-20 under 35 U.S.C. § 102(b) has been overcome and that all claims pending herein are in condition for allowance.

Allowable Subject Matter

Applicants gratefully acknowledge the Examiner's indication of allowable subject matter in claims 1 through 15, stating that such claims would be allowable if rewritten to overcome the Examiner's rejection under 35 U.S.C. § 112, 2nd paragraph.

Applicants respectfully submit that claims 1 and 15 have been amended to correct the deficiencies noted by the Examiner under 35 U.S.C. § 112 2nd paragraph. Therefore, the Examiner's rejection has been overcome and claims 1-15 are in condition for allowance.

Prior Art Made of Record

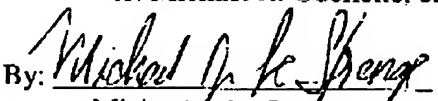
The prior art made of record by the Examiner and not relied upon, i.e. Nozawa, et al. (U.S. Patent No. 5,459,423); Merrit (U.S. Patent No. 5,583,463); Kato (U.S. Patent No. 5,907,513); Cutter. Et al. (U.S. Patent No. 6,255,894); Kim, et al. (U.S. Patent No. 6,489,832); Lim, et al. (U.S. Patent No. 6,498,526); Mori, et al. (U.S. Patent No. 6,566,937); Jung (U.S. Patent App. No. 2004/0046601); Huang (U.S. Patent App. No. 2005/0151578); Wallstab (U.S. Patent No. 6,933,742); Parker, et al. (U.S. Patent App. No. 2005/0212584); and Newman (U.S. Patent App. No. 2005/0285663), have been reviewed and Applicants respectfully submit that the references cited do not anticipate or suggest the elements of pending independent claims 1, 15 and 16.

Conclusion

Based on the foregoing, it is respectfully submitted the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,
For: Michael R. Ouellette, et al.

By: 

Michael J. Le Strange
Registration No. 53,207
Telephone No.: (802) 769-1375
Fax No.: (802) 769-8938
EMAIL: lestrang@us.ibm.com

International Business Machines Corporation
Intellectual Property Law - Mail 972E
1000 River Road
Essex Junction, VT 05452